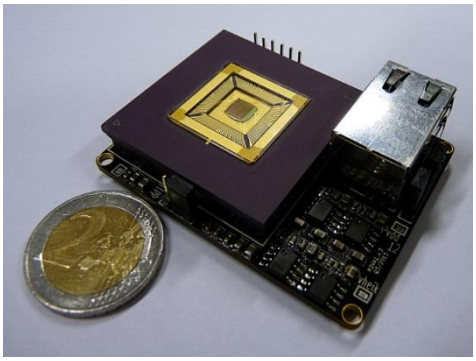
KOVA1 sensor-processor IC and embedded camera system

Technical overview

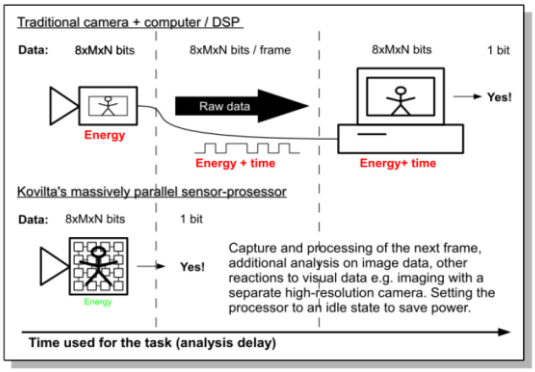
Embedded camera system

- Kovilta's proprietary pixel-parallel sensor-processor IC
- Compact, single-PCB embedded system with Xilinx FPGA for program control and I/O
- Ethernet connectivity, Power-over-Ethernet
- PC software (KEDE) for programming-, control- and data acquisition can receive input from multiple cameras
- Autonomous camera operation with onboard nonvolatile memory and FPGA control, no on-line PC-connection necessary during processing
- Data readout to any device with Ethernet connectivity or directly via PCB pins (e.g. fast trigger signal output)



KOVA1 sensor-processor chip architecture

- Processor-per-pixel array implementing massively parallel sensor-level image content analysis
- Simultaneous processing of each pixel of the image with continuous access to the local neighborhood pixel values
- Pixel-level memory for storing image frames and intermediate processing results locally
- Pixel-level A/D/A conversion, digital pixel I/O
- Programmable pixel-level grayscale and binary (1-bit) processing circuitry employing analog and digital (mixed-mode) circuit techniques for optimal efficiency
- Additional peripheral logic for array-leve analysis and image data-dependent program control



No data transfer delay between image capture with sensor front-end and low-level image analysis

Pixel-parallel processing leads to very high analysis performance and very good power efficiency

Programmable pixel processor elements with local memory enable complex analysis on a single chip

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SENSORS WITH SENSE

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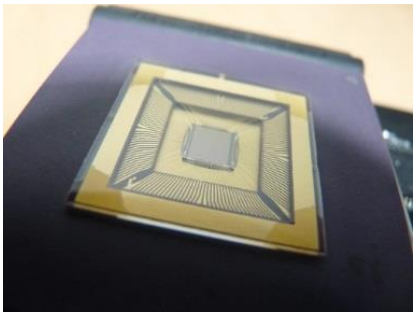
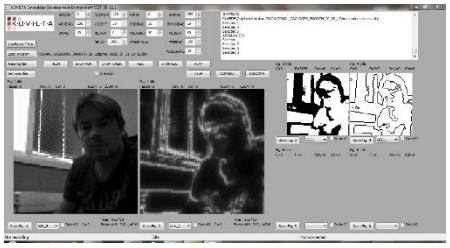


KOVA1 IC technical data

- Full-custom ASIC by Kovilta
- 96x96 pixel sensor-processor array
- 180 nm (1P6M) mixed-mode CMOS technology
- Chip area: 5x5 mm^2, area per pixel cell: 41x41 μm^2
- Each pixel cell includes a 10x10 μm^2 sensor diode
- Scalable to 256x256 pixel resolution within 1 cm^2 IC area
- Program controller can be integrated on the same chip

Pixel-level functionality

- Real-time compression of image dynamic range via on-line processing during image capture
- Pixel neighborhood connectivity: 1. or 2. neighborhood
- Local memory: 4 x grayscale (dynamic), 19 x binary (static), static grayscale storage possible via pixel-level A/D/A loop
- Analog preprocessing of grayscale data: linear and nonlinear filtering, mathematical morphology, analog arithmetic
- Programmable processing of 1-bit data: basic logic operations, neighborhood threshold logic, mathematical morphology, asynchronous trigger-wave propagation, etc.
- Pixel-level control feedback between binary object-level analysis results and grayscale segmentation



Peripheral logic functionality

- Automatic pixel counting (row/colum/global sum), and coordinate extraction
- Region-of-interest operations (read/write)
- Histogramming and object-parallel feature comparison

Pixel-level analysis up to 100000 fr/s, depending on algorithm complexity and imaging conditions

Minimal processing latency enables external reaction to analysis results in < 1 us

Massively parallel local processing offers a computing efficiency of > 100 GOPS/W

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